

In the Claims:

Please cancel Claims 1-18 without prejudice or disclaimer.

Please amend claims 19 and 23-26 as follows.

Claims 1-18. (Canceled).

19. (Currently Amended) A NOR logic circuit having a first input and a second input comprising:

a semiconductor substrate;

an insulator formed on said semiconductor substrate;

a semiconductor layer formed on said insulator;

a p-well formed in said semiconductor layer;

a first gate structure formed atop said p-well, said first gate structure being the first input and being formed from a thin gate oxide layer underneath a conductive layer;

a second gate structure formed atop said p-well, said ~~first~~ second gate structure being the second input and being formed from a thin gate oxide layer underneath a conductive layer;

a n- base formed adjacent to a first edge of said first gate structure and said second gate structure;

a p+ structure formed within said n- base;

a second p+ structure adjacent to a second edge of said first gate structure and said second gate structure, said second p+ structure being the output of said NOR logic circuit;

a first switch formed in said semiconductor layer, said first switch electrically connected to said first input; and

a second switch formed in said semiconductor layer in series to said first switch and electrically connected to said second input, said second switch also electrically connected to said second p+ structure.

20. (Original) The NOR gate of Claim 19 wherein said p-well extends through said semiconductor layer to said insulator.
21. (Original) The NOR gate of Claim 19 wherein said p+ structure and said n+ structure extend through said semiconductor layer to said insulator.
22. (Original) The NOR of Claim 19 wherein said semiconductor layer is less than 1500 angstroms thick.
23. (Currently Amended) A NOR logic circuit having a first input and a second input comprising:
- a semiconductor substrate;
  - an insulator formed on said semiconductor substrate;
  - a semiconductor layer formed on said insulator;
  - a n- well formed in said semiconductor layer, said n-well being the output of said NOR gate;
- a first gate structure formed atop said n-well, said first gate structure being the first input and being formed from a thin gate oxide layer underneath a conductive layer;
- a second gate structure formed atop said n-well, said first second gate structure being the second input and being formed from a thin gate oxide layer underneath a conductive layer;
- a[[n]] p+ structure formed adjacent to a first edge of said first gate structure and said second gate structure;
- a second p+ structure adjacent to a second edge of said first gate structure and said second gate structure, said second p+ structure being the output of said NOR logic circuit;
- a first switch formed in said semiconductor layer, said first switch electrically connected to said first input; and
- a second switch formed in said semiconductor layer in series to said first switch and electrically connected to said second input, said second switch also electrically connected to said second p+ structure.

24. (Currently Amended) The NOR logic circuit NAND gate of Claim 23 wherein said n-well extends through said semiconductor layer to said insulator.
25. (Currently Amended) The NOR logic circuit NAND gate of Claim 23 wherein said first p+ structure and said second p+ structure extend through said semiconductor layer to said insulator.
26. (Currently Amended) The NOR logic circuit NAND gate of Claim 23 wherein said semiconductor layer is less than 1500 angstroms thick.